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VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

[Central Technological Institute, Maharashtra State]

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SEMESTER EXAMINATION	***May 2013***	DATE OF EXAM	20/5/2013
SEMESTER & PROGRAM	***IV S. Y. B. Tech (Computer)***	TIME	1.30PM - 4.30PM
TIME ALLOWED	***3 HRS.***	MARKS	***100***
COURSE (Course Code) :	***CO0206- COMPUTER ORGANIZATION,ASSEMBLY & MAINTENANCE***		

Instructions
1. All questions are compulsory. Internal choice is indicated wherever applicable.
2. Figures to the right indicate full marks.
3. Sub questions of individual question should be written one below the other.

Q.1 **All the following objective questions are compulsory.**

a. List & briefly define the possible states that define an instruction execution. 4

b. What are the four main components of any general purpose computer? 2

c. What general categories of functions are specified by computer instructions? 2

d. What types of operands are typical in machine instruction sets? 2

e What are the two basic tasks of control unit 2

f The size of a block in Directly Mapped cache is 1024 bytes and the number of lines in the cache is 64. What would be the size of the cache. 2

g How would you interpret the following control signal: 2

$C5 = \overline{P}\,\overline{Q}\,T2 + \overline{P}.Q.T2$,
where P, Q : $0,0 \rightarrow Fetch$, $0,1 \rightarrow Indirect$, $1,0 \rightarrow Execute$, $1,1 \rightarrow Interrupt\ cycle$.

h Write the micro-operations for Indirect cycle. 2

i List any 4 motherboard fault symptoms. 2

Q.2 a. Explain virtual memory concept with reference to paging & segmentation 10

OR

Discuss different parallel computer structures

b. Explain Booth's algorithm with flowchart & example 10

Q3 **Attempt all the sub-questions.**

A Draw the motherboard Logic diagram in a single board microcomputer 6

B With appropriate diagrams explain **any 2** of the following in 8284 clock generator 6
1) Clock Logic 2) Reset Logic 3) Ready Logic.

C With a diagram explain the motherboard DMA Logic. Explain the Idle and Active Cycles in 8237 DMA Controller. 6

Q4 Attempt any 3 from the following sub-questions

A Name any 4 approaches of dealing with conditional branches. Name the various techniques in branch prediction. Draw the Branch Prediction flowchart. 7

B Define Instruction Cycle Code (ICC). Explain control signals and data paths with a diagram relevant to suitable micro-operations of your choice. 7

C Draw the horizontal microinstruction format. How is a microinstruction interpreted? Draw a diagram of the organization of control memory. 7

D Name the 3 micro-instruction sequencing techniques. Explain any one with suitable diagram. 7

Q5 Attempt any 3 of the following sub-questions

A What are the 2 design issues in interrupt I/O implementation? Name the 4 techniques in device identification that cause interrupts and explain any 2? 7

B Define 1) Stripe 2) Strip in RAID Systems. Explain the Winchester disk format with appropriate diagram. 7

C Draw a DRAM memory cell diagram. Design the chip logic block diagram for 16MB DRAM with 11 address lines. 7

D What are the 4 main reasons memory references tend to cluster? What are spatial and temporal localities of references. 7