VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

[Central Technological Institute, Maharashtra State]

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SEMESTER EXAMINATION	***May 2013***	DATE OF EXAM	
SEMESTER & PROGRAM	***IV S. Y. B. Tech (Computer)***	TIME	
TIME ALLOWED	***3 HRS.***	MARKS	***100***
COURSE (Course Code) :	***CO0206- COMPUTER ORGANIZATION ASSEMBLY & MAINTENANCE***		

Instructions
1. All questions are compulsory. Internal choice is indicated wherever applicable.
2. Figures to the right indicate full marks.
3. Sub questions of individual question should be written one below the other.

Q.1 **Attempt all the following objective type sub-questions.** 20

a. Give Sign-Magnitude Two complement representation of the following 4-bit integer (represented in decimal format) 2
-1, -7

b. What are typical elements of a machine instruction? 2

c. List and briefly define two approaches to deal with multiple interrupts. 2

d. What do you understand by Computer architecture & Computer organization? Give examples of architectural attributes & Organizational attributes. 4

e Define Unit of Transfer in memory systems. List the performance parameters for memory systems. 2

f The size of a block in Directly Mapped cache is 1024 bytes and the number of lines in the cache is 64. What would be the size of the cache? 2

g How would you interpret the following control signal: 2

$C5 = \bar{P}.\bar{Q}.T2 + \bar{P}.Q.T2$,
where P, Q 0,0 $\rightarrow$ *Fetch*, 0,1 $\rightarrow$ *Indirect*, 1,0 $\rightarrow$ *Execute*, 1,1 $\rightarrow$ *Interrupt cycle.*

h Write the micro-operations for Execute cycle. 2

g What are Layman's checks? List any 4 Layman's checks. 2

Q.2 a Give Flynn's Classification of parallel processing systems. 8

OR

What is "Virtual Memory"? Explain "paged virtual memory system".

b. Explain why multiple bus hierarchies are required. Explain traditional bus architecture and High performance bus architecture. 10

c. Give block diagram of hardware for Addition and Subtraction using two's complement representation. 2

OR

Give Instruction cycle state diagram

Q3 Attempt all the following sub-questions.

A Draw the motherboard Logic diagram in a single board microcomputer 6

B With appropriate diagrams explain **any 2** of the following in 8284 clock generator: 1) Clock Logic 2) Reset Logic 3) Ready Logic in. 6

C With a diagram explain the motherboard Interrupt Logic. Draw a block diagram for 8259 Interrupt Controller. 6

Q4 Attempt any 3 from the following sub-questions

A Name any 4 approaches of dealing with conditional branches. Draw a block diagram for the Branch History Table strategy in branch prediction. 7

B Define Instruction Cycle Code (ICC). With a model block diagram explain the Inputs and Outputs of Control Unit. 7

C Define: 1) Micro-instruction 2) Control Word. With a block diagram explain the functioning of micro-programmed control unit. 7

D Name the 3 micro-instruction sequencing techniques. Explain any one with suitable diagram. 7

Q5 Attempt any 3 of the following sub-questions

A Draw the flowcharts of 3 techniques (Programmed, Interrupt driven and DMA) for input of block of data. Explain memory mapped I/O and isolated I/O 7

B Define 1) Stripe 2) Strip in RAID Systems. Explain the CD-ROM block format with appropriate diagram. 7

C List any 3 differences between SRAM and DRAM. Design the chip logic block diagram for 16MB DRAM with 11 address lines. 7

D What are the 4 main reasons memory references tend to cluster? What are spatial and temporal localities of references? 7