VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

[Central Technological Institute, Maharashtra State]

Matunga, Mumbai-400 019

SEMESTER EXAMINATION	*May 2009*	DATE OF EXAM	*7th May 2009*
SEMESTER & COURSE	*IV S Y B Tech Eletrx*	TIME	*2.30 p.m. To 5.30 p.m.*
TIME ALLOWED	*3 HRS.*	MARKS	*100*
SUBJECT :	*ELECTRICAL NETWORK ANALYSIS*		

Instructions:
1. Attempt Any Five Questions.
2. Figures to the right indicate Full Marks.
3. Assume suitable **additional data**, if required.
4. Illustrate your answer with neat sketches whenever necessary.

Q1. a) Replace the network of Fig Q1 (a) at terminal a-b with a Notron's equivalent and Thevenin's Equivalent network. (10)

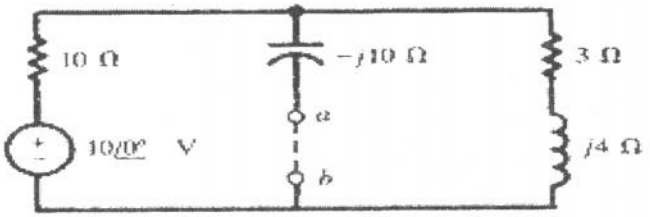

Fig Q1 (a)

b) Determine the voltage across 20 Ω resistor in the following circuit with the help of Superposition theorem. (Fig Q1 (b)) (10)

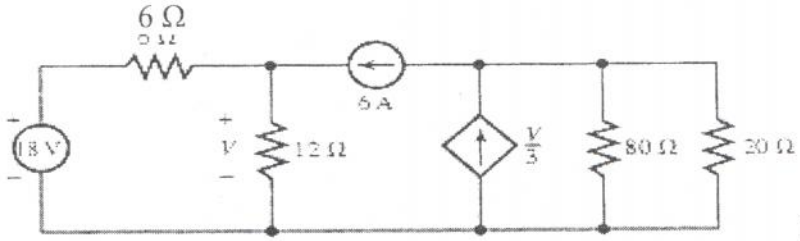

Fig Q1 (b)

Q2 (a) For the circuit shown in Fig Q2(a) draw oriented graph and write i) Incidence matrix, ii) F cutest matrix, iii) Tie set matrix. (10)

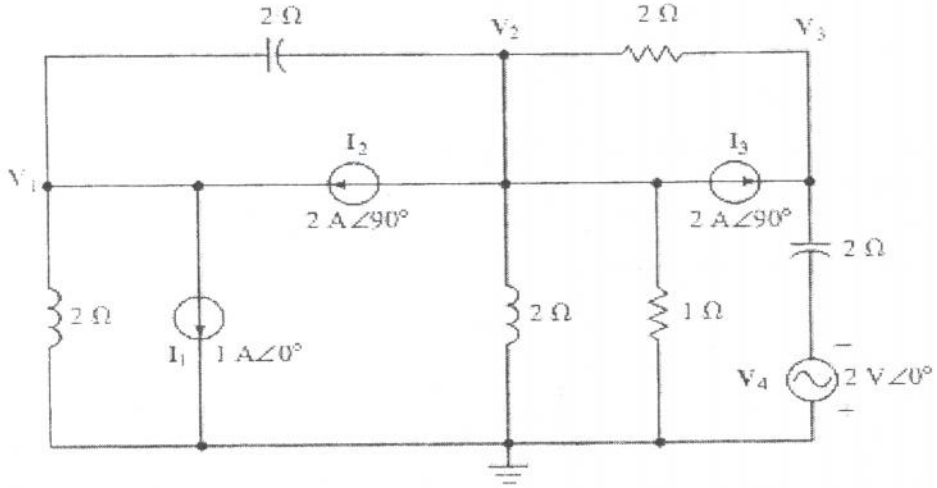

Fig Q2 (a)

b) For the network shown prove that $AB^T = 0$. (10)

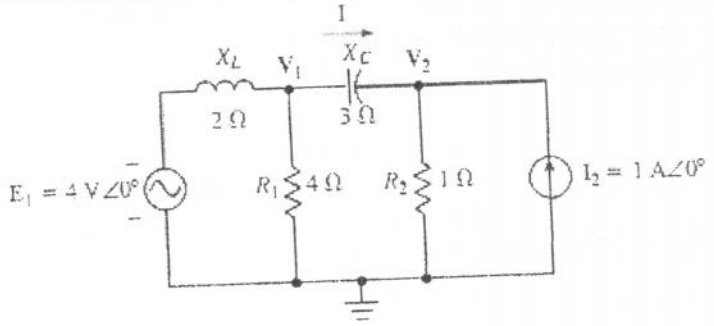

Fig Q2 (b)

Q3 a) Determine i_L (t) for t > 0. the circuit of Fig Q3 (a). (10)

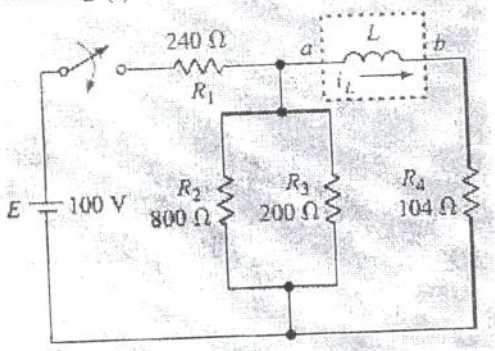

Fig Q3 (a)

b) Find i, di/dt, di^2 / dt^2 for the network shown in Fig Q3 (b). (10)

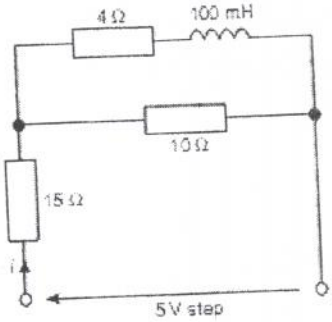

Fig Q3 (b)

Q4 a) For the circuit shown find i(t) for t > o using Laplace Transform. The switch is closed at t = 0. (10)

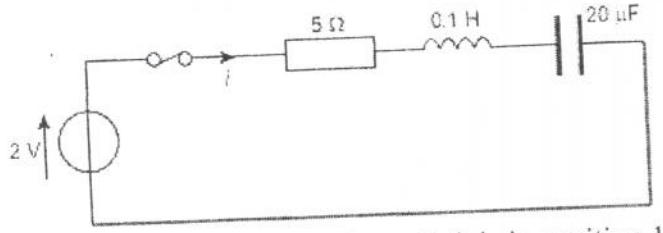

Fig Q4 (a)

b) In the R-L circuit shown the switch is in position 1 long enough to establish steady state conditions, and at t = 0 it is in position 2, Find i(t) for t > 0 using Laplace transform. (10)

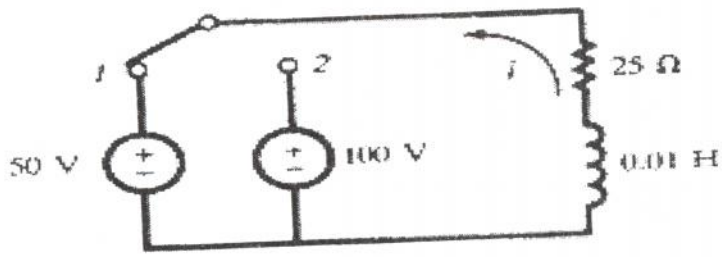

Fig. Q4 (b)