VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

[Central Technological Institute, Maharashtra State]

Matunga, Mumbai-400 019

SEMESTER EXAMINATION	*May 2009*	DATE OF EXAM	*13th May 2009*
SEMESTER & COURSE	*IV S Y B Tech Eletrx*	TIME	*2.30 p.m. To 5.30 p.m.*
TIME ALLOWED	*3 HRS.*	MARKS	*100*
SUBJECT :	*DIGITAL DESIGN - II*		

Instructions: 1. All Questions are Compulsory.
2. Figures to the right indicate full marks.
3. Draw neat diagram wherever necessary.
4. Assume suitable data

Q.1) A) Analyze the clocked synchronous state machine in fig.1 given below. Write excitation equation, transition equation, transition table and state or output table. Draw state diagram and draw timing diagram for CLK, EN, Q1and Q0 for 10 clock ticks assuming that the machine starts in state 00 and EN is continuously 1. **(10)**

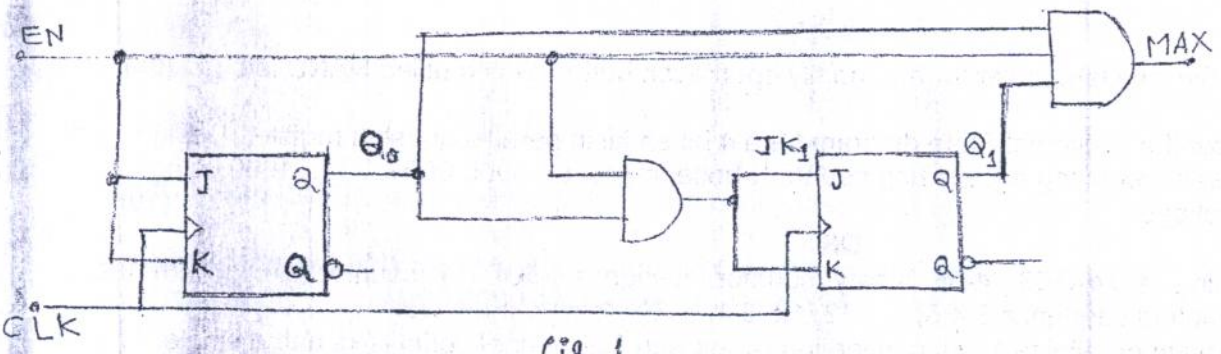

fig. 1

B) a) Draw timing diagram for a NOR latch showing each of the following sequences of events.

i) S & R are both HIGH, S goes LOW before R.
ii) S & R are both HIGH, R goes LOW before S.
iii) S & R are both HIGH, S & R go LOW Simultaneously,
b) State why S=R= 1, is a forbidden state for the NOR latch.
c) Briefly explain what the final result is for each of the transition listed in part of this question. **(06)**

C) Differentiate between synchronous and asynchronous counters. **(04)**

Q.2) A) The Moore Machine has one input ***w*** and one output ***z***. All changes in circuit occur on the positive edge of a clock signal. The output ***z =1.*** if during two immediately preceding clock cycle the input ***w*** was equal to one, otherwise the value ***z =0***. Design a circuit for this machine.

OR

A) A state machine called a single-pulse generator operates as follows.
a) The circuit has two states ***seek*** and ***find*** an input called ***sync*** and an output called ***pulse***.
b) The state machine resets to the state ***seek***. If ***sync = 1*** the machine remains in ***seek*** and the output ***pulse*** remains LOW.
c) When ***sync = 0*** the machine makes a transition to ***find***. In this transition ***pulse*** goes HIGH.

d) When the machine is in state ***find*** and ***sync = 0***, the machine remains in ***find*** & ***pulse*** goes LOW.

e) When the machine is in state ***find*** and ***sync = 1*** the machine goes back to ***seek*** and ***pulse*** remains LOW.

i) Draw state diagram.

ii) Use classical state machine design technique to design, the circuit for the single pulse generator using D FF for the state logic. **(10)**

B) Is the state machine in fig.2, a Moore machine or a Mealy machine? Explain your answer. **(05)**

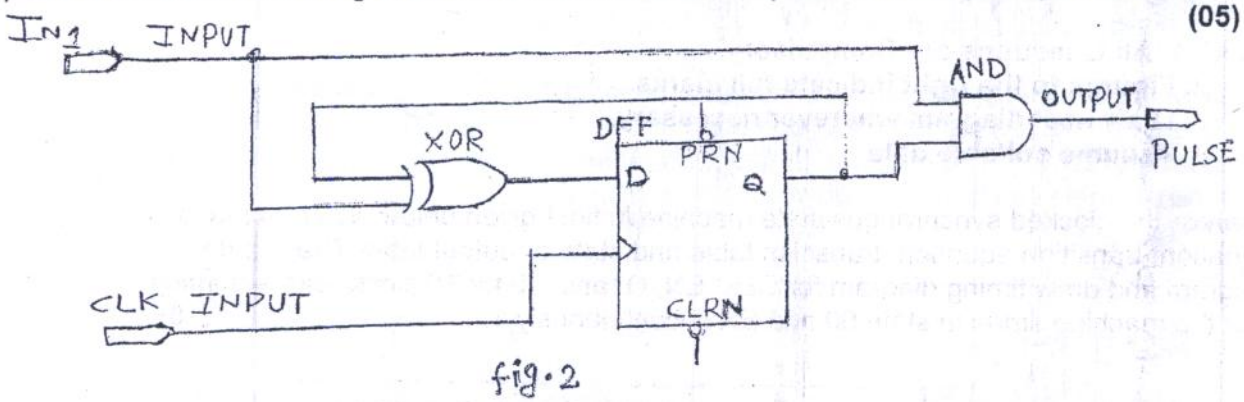

fig. 2

C) Explain Switch Debouncer for a normally open push button switch using NAND latch? **(05)**

Q.3) A) Draw the Universal State diagram for a 4 bit serial in parallel out shift register. Design a 4-bit self correcting twisted ring counter whose states are 0000,0001,.....,1000 using MSI package. **(10)**

OR

A) Using a 74X163, 4-bit binary counter, design a MOD-11 counter circuit with the counting sequence 3,4,5,.....12, 13, 3,4,.....Explain your answer.

B) Explain parallel to serial conversion circuit with 32-channel serial links and a single 2.048 MH_z, 8 bit parallel data bus that carries 256 bytes per frame. Show the timing of the parallel bus and the serial bus timeslots are transmitted on serial links. Draw logic diagram for the circuit using MSI IC. **(10)**

Q.4) A) Draw the state diagram for the given state table. Reduce the state table if possible and obtain state diagram and new state table. **(10)**

P.S	N.S/ OUTPUT	
	X = 0	X =1
a	f,0	b,0
b	d,0	c,0
c	f,0	e,0
d	g,1	a,0
e	d,0	c,0
f	f,1	b,1
g	g,0	h,1
h	g,1	a,0

B) Discuss Xilinx XC9500 CPLD architecture.

OR

B) Discuss ROM memory and connection to build the 2 to 4 decoder using 8x4 ROM. **(10)**