VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

[Central Technological Institute, Maharashtra State]

MATUNGA, MUMBAI- 400019

SEMESTER EXAMINATION	: May 2012	DATE OF EXAM	: 18 /05/2012
SEMESTER & PROGRAM	: IV S.Y.BTech	MARKS	: 100
TIME ALLOWED	: 3 HRS.	TIME	: 1:30p.m. – 4:30p.m.
COURSE (Course Code)	: **Electronics and Communication Systems**		

Instructions

1 All questions are compulsory.
2 All questions carry equals marks.
3 Figures to the right indicate full marks.
4 All sub-questions must be written together.

Q.1	a	(i)	What is Punch Through Effect?	2M
		(ii)	What do you understand by 'Pinch off voltage' and 'Cut off voltage'?	2M
		(iii)	Perform BCD Addition for $(9)_{10}+(8)_{10}$	2M
		(iv)	Perform BCD Subtraction for $(6)_{10}-(3)_{10}$	2M
		(v)	Subtract using 2's Complement Method $(7)_{10}-(2)_{10}$	2M
	b	(i)	Explain characteristics of a Practical OP-AMP.	5M
		(ii)	Write short note on: Race around condition in JK flip-flop.	5M
Q.2	a		Draw and explain the input and output characteristics of a transistor in CE configuration. Indicate Cut-Off, Saturation & Active regions.	10M
	b		Draw a circuit for obtaining drain and transfer characteristics for an n-channel JFET, and explain how to get values to plot the said characteristics.	10M
			OR	
	c		Explain the various op-amp Open Loop Configurations.	5M
			Convert 4 Bit Binary number to 4 Bit Gray. Design logic circuit for the same.	5M
Q.3	a		Draw the A.C. equivalent circuit for the Single input balanced output differential amplifier and derive the expressions for the differential input resistance, output resistance and voltage gain for the same.	10M
	b		For the Dual input unbalanced output differential amplifier the various circuit parameters are $\|VCC\|=\|VEE\|=10v$, $R_C=4.7K\Omega$, $R_{S1}=R_{S2}=50\ K\Omega$, $R_E=6.8K\Omega$. (i)Calculate Q point values. (ii)Calculate voltage gain. (iii)Obtain input and output resistance values. (iv)Determine the output voltage Vo if $V_{S1}=50mV$ (p-p). Assume $\beta_{ac}=\beta_{dc}=50$, $V_{BE}=0.7$	10M
Q.4	a		Simply the following expression using K-Map. Design the logic circuit for the same. (i)$F(A, B, C, D)=\sum m\ (1, 3, 7, 8, 10, 12, 13, 15)$ (ii)$F(A, B, C, D)=\prod M(0, 5, 7, 8, 9, 10, 11, 13)$	10M

P.T.O

Q.4 b Explain with a neat diagram Phase discriminator (foster-seeley). 10M

OR

How is Adaptive Delta Modulation better than Linear Delta Modulation? Draw block diagram of adaptive delta modulation and explain each block in detail. 10M

Q.5 a Draw a block diagram of high quality superhetrodyne communication receiver and describe function of each block. 10M

Q.5 b A chemical reactor has three sensor indicating the following conditions: 10M

(i) Pressure 'P' is low or high.
(ii)Temperature 'T' is low or high.
(iii)Liquid level 'L' is low or high.
H has two controls: Heater (H) which is either On or Off & an Inlet Valve (V) which is either Open or Closed.
The controls are operated as shown in the table.
(a)Using the convention HIGH=1, LOW=0, ON=1, OFF=0, OPEN=1, CLOSED=0 & SHUT DOWN=0. Draw the K-Map for H & V.
(b)Obtain the minimal SOP and POS Expressions for H & V.
(c)Replace The Logic H & V by using Logic Gates.

INPUTS			OUTPUTS	
P	T	L	H	V
LOW	LOW	LOW	OFF	OPEN
LOW	LOW	HIGH	ON	CLOSED
LOW	HIGH	LOW	OFF	OPEN
LOW	HIGH	HIGH	OFF	CLOSED
HIGH	LOW	LOW	ON	OPEN
HIGH	LOW	HIGH	ON	CLOSED
HIGH	HIGH	LOW	OFF	CLOSED
HIGH	HIGH	HIGH	X	X